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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/808,114	03/15/2001	Leonard Forbes	M4065.0381/P381	3126

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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/808,114	Applicant(s) FORBES ET AL.
	Examiner Kevin Quinto	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-67* is/are pending in the application.

4a) Of the above claim(s) *68-91* is/are withdrawn from consideration.

5)☒ Claim(s) *17-32 and 54-67* is/are allowed.

6)☒ Claim(s) *1,2,4-10 and 33-45* is/are rejected.

7)☒ Claim(s) *3,11-16 and 46-53* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Claims 68-91 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 8.

Claim Objections

2. Claim 37 is objected to because of the following informalities: "nitrided oxyide" should be spelled nitrided oxide. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 33-41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 33 recites the limitation "said three vertical gate electrodes" in the second half of the claim. There is insufficient antecedent basis for this limitation in the claim.

6. Claims 40 and 41 recite the limitation "the central gate electrode." There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

8. Claims 1, 2, 4-6, 33, 34, 40, and 41 are rejected under 35 U.S.C. 102(e) as being anticipated by Mandelman et al. (USPN 6,097,070).

9. In reference to claim 1, Mandelman et al. (USPN 6,097,070, hereinafter referred to as the "Mandelman" reference) discloses a similar device. Figure 2 of Mandelman illustrates a semiconductor device with a substrate having at least two spaced apart doped source/drain regions (21) with a channel region between them. There is a transistor gate with a first gate electrode (25) over the substrate and between the spaced apart doped source/drain regions (21). There are two second gate electrodes (26) located on either side of the first gate electrode (25). The two second gate electrodes (26) are separated from the first gate electrode (25) by an insulating dielectric layer (29). The first gate electrode (25) is of a first conductivity type and the two second gate electrodes (26) are of a second conductivity type.

10. With regard to claim 2, there is a conductive cap layer (23) electrically connecting the first (25) and second gate electrodes (26).

11. In reference to claims 4 and 5, Mandelman discloses these conductivity types in figure 2 and in column 4, lines 35-49.

12. With regard to claim 6, Mandelman discloses the use of doped polysilicon in column 4, lines 35-49.

13. So far as understood in claim 33, Mandelman discloses a similar device. Figure 2 of Mandelman illustrates a semiconductor transistor with three gate electrodes (25, 26) over a substrate and at least partially between two spaced apart doped source/drain regions (21). There is a center gate electrode (25) of p+ type conductivity and two adjacent outer gate electrodes (26) of n+ type conductivity. There is a gate dielectric (27) separating the three gate electrodes (25, 26) from the substrate. A thin dielectric layer (29) separates the outer gate electrodes (26) from the center gate electrode (25). A conductive cap layer (23) is over the three gate electrodes (25, 26). The conductive cap layer (23) electrically connects the three gate electrodes (25, 26). There are insulating sidewalls (22) adjacent to the conductive cap layer (23) and the outer gate electrodes (26).

14. So far as understood in claim 34, Mandelman discloses the use of doped polysilicon in column 4, lines 35-49.

15. So far as understood in claims 40 and 41, Mandelman discloses (in column 3, lines 15-26) that there is a work function difference between the center gate electrode (25) and the outer gate electrodes (26) which leads to the center gate electrode (25) having a higher threshold voltage than the outer gate electrodes (26).

16. Claims 42-45 are rejected under 35 U.S.C. 102(e) as being anticipated by Yu (USPN 6,348,387 B1).

17. In reference to claim 42, Yu (USPN 6,348,387 B1) discloses a similar device. Figures 10-12 of Yu illustrate a semiconductor device with a substrate (204) having at least two spaced

apart doped source/drain regions (234, 232) with a channel region between them. There is a gate dielectric (212) over the substrate (204). There is a central gate (214) over the channel region and the gate dielectric (212). There are two outer gate electrodes (222, 224) located over the channel region and the gate dielectric (212) and adjacent to the central gate electrode (214). The two outer gate electrodes (222, 224) are separated from the central gate electrode (214) by a dielectric layer (226, 228). Yu discloses (column 6, lines 39-45) that the central gate electrode (214) has a greater threshold voltage than the outer gate electrodes (222, 224).

18. With regard to claim 43, Yu discloses (column 6, lines 45-51) that source and drain extensions (264, 262) or virtual source/drain junctions form when a voltage is applied to the outer gate electrodes (222, 224).

19. In reference to claim 44, figures 10-12 of Yu show a conductive cap (256) which electrically connects the central (214) and outer (222, 224) gate electrodes.

20. With regard to claim 45, Yu discloses (column 6, lines 52-57) the use of a metal central gate electrode (214) which has a work function higher than that of the outer gate electrodes (222, 224).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mandelman et al. (USPN 6,097,070) in view Naruse et al. (USPN 5,356,821).

23. In reference to claim 7, Mandelman does not disclose the use of silicon germanium in the first gate electrode. However the use of silicon germanium in gate electrodes is well known in the art. Naruse et al. (USPN 5,356,821, hereinafter referred to as the "Naruse" reference) discloses that a silicon germanium gate, due to its low resistivity, allows a transistor to have a faster operation speed (column 4, lines 23-30). Naruse discloses that transistors with fast operation speeds are desirable in the art (Background of the Invention). It would therefore be obvious to use silicon germanium as the material for the first gate electrode in the device of Mandelman in order to attain a device with a faster operation speed.

24. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mandelman et al. (USPN 6,097,070) in view Forbes et al. (USPN 5,886,368).

25. In reference to claim 8, Mandelman does not disclose the use of silicon carbide or silicon oxycarbide in the first and second gate electrodes. However the use of silicon oxycarbide in gate electrodes is well known in the art. Forbes et al. (USPN 5,886,368, hereinafter referred to as the "Forbes" reference) discloses that the use of silicon oxycarbide as a gate material allows an adjustment of the barrier between the gate and the gate dielectric (column 2, lines 39-47). Forbes discloses that tailoring the barrier between the gate and the gate dielectric is desired in the art (column 2, lines 22-32 and column 5, lines 38-51). It would therefore be obvious to use silicon oxycarbide as the material for the first and second gate electrodes in the device of Mandelman in order to allow an adjustment of the barrier between the gate and the gate dielectric.

26. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mandelman et al. (USPN 6,097,070) in view of Wilk et al. (USPN 6,274,510 B1).

27. With regard to claims 9 and 10, Mandelman discloses that the dielectric layer (29) is used as a diffusion barrier (column 3, lines 46-52). Mandelman does not disclose the use of a nitride as the dielectric layer (29). However the use of a nitride as a diffusion barrier is well known in the art. Wilk et al. (USPN 6,264,510 B1, hereinafter referred to as the "Wilk" reference) discloses that silicon nitride is an effective diffusion barrier with regard to boron and other dopants (column 1, lines 55-57). Wilk further states that this property helps to limit dopant depletion from polysilicon gates (column 1, lines 57-59) which Mandelman states is a desired property for the dielectric layer (Mandelman, column 3, lines 46-52). It would therefore be obvious to use silicon nitride as the dielectric layer in the device of Mandelman since it limits dopant depletion from polysilicon gates.

28. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mandelman et al. (USPN 6,097,070) in view Naruse et al. (USPN 5,356,821).

29. So far as understood in claim 35, Mandelman does not disclose the use of silicon germanium in the center gate electrode. However the use of silicon germanium in gate electrodes is well known in the art. Naruse (USPN 5,356,821) discloses that a silicon germanium gate, due to its low resistivity, allows a transistor to have a faster operation speed (column 4, lines 23-30). Naruse discloses that transistors with fast operation speeds are desirable in the art (Background of the Invention). It would therefore be obvious to use silicon germanium as the material for the center gate electrode in the device of Mandelman in order to attain a device with a faster operation speed.

30. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mandelman et al. (USPN 6,097,070) in view Forbes et al. (USPN 5,886,368).

31. So far as understood in claim 36, Mandelman does not disclose the use of silicon carbide or silicon oxycarbide in the three gate electrodes. However the use of silicon oxycarbide in gate electrodes is well known in the art. Forbes (USPN 5,886,368) discloses that the use of silicon oxycarbide as a gate material allows an adjustment of the barrier between the gate and the gate dielectric (column 2, lines 39-47). Forbes discloses that tailoring the barrier between the gate and the gate dielectric is desired in the art (column 2, lines 22-32 and column 5, lines 38-51). It would therefore be obvious to use silicon oxycarbide as the material for the three gate electrodes in the device of Mandelman in order to allow an adjustment of the barrier between the gate and the gate dielectric.

32. Claims 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mandelman et al. (USPN 6,097,070) in view of Wilk et al. (USPN 6,274,510 B1).

33. So far as understood in claims 37 and 38, Mandelman discloses that the dielectric layer (29) is used as a diffusion barrier (column 3, lines 46-52). Mandelman does not disclose the use of a nitride as the dielectric layer (29). However the use of a nitride as a diffusion barrier is well known in the art. Wilk (USPN 6,264,510 B1) discloses that silicon nitride is an effective diffusion barrier with regard to boron and other dopants (column 1, lines 55-57). Wilk further states that this property helps to limit dopant depletion from polysilicon gates (column 1, lines 57-59) which Mandelman states is a desired property for the dielectric layer (Mandelman, column 3, lines 46-52). It would therefore be obvious to use silicon nitride as the dielectric layer in the device of Mandelman since it limits dopant depletion from polysilicon gates.

Allowable Subject Matter

34. Claims 17-32 and 54-67 are allowed.

35. Claims 3, 11-16, and 46-53 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

36. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of semiconductor device with three doped gates (laterally isolated from each other), two of which are of a first conductivity type and the other being of the opposite conductivity type which are formed directly over a channel which is between the source and drain regions.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (703) 306-5688. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KVQ
November 27, 2002

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